Simulink Documentation

Part 1: For all implemented components you will need to document your design and implement the design in Simulink.

Document the design as follows:

1. List all requirements. This should be done formally (as in not just a bunch of bullet points), but as a group you can decide what formalism you want to use (mathematical, informal, somewhere in between).
2. Requirements must be concise and disjoint. They should also be traceable to the design and vice versa
3. List all design decisions.
4. The Simulink diagram must include necessary annotation to understand the model. There should be screenshots of the simulink model in the documentation. Provide an additional section in the document that describes testing you performed, and the results.

This document defines the functions and operating characteristics that the system must perform and provides a description of the system's environmental performance parameters and critical interactions.

# Part 1: Requirements and design

## Requirements

These are all the requirements for the Simulink implementation of the pacemaker and its modes.

### Overall Pacemaker System

The pacemaker should provide rate adaptive bradycardia pacing support, historical data on device implementation, and user diagnostics through brady analysis function. In addition, the bradycardia analysis functions should allow pacing measurements such as lead impedance, pacing threshold, P and R wave measurement, battery status, temporary brady pacing, motion sensor trending, and tests to be performed.

### Device Operation

* The device should monitor and handle a patient's heart rate by detecting and providing therapy for bradycardia.
* The device should provide programmable, single-chamber, rate-adaptive pacing, and permanent state.
* The device should be programmed and controlled through the Device Controller-Monitor (DCM).
* The device should provide history data such as output rate histograms (atrial and ventricular) and sensor output data.

### Pulse Pacing (Atrial and Ventricular)

The device should result in pulses with programmable voltages and widths for atrial and ventricular, which provide electrical heart-pacing stimulation.

### Amplitude and Width

Both amplitude and width for pulse pacing should be independently programmable .

### Rate Sensing

Bipolar electrodes and a sensing circuit should operate rate sensing. Rate detection should be based on the measured cardiac cycle measurements of the sensed rhythm and assessed on an interval-by-interval basis.

### Operation Modes

The DCM will be used to select a permanent operating mode for the pacemaker at startup. At present, it will choose between the modes AOO, VOO, AAI, and VVI.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | LRL | URL | Atrial |  |  |  |  |  |  |
| AOO | O | O |  |  |  |  |  |  |  |
| VOO | O | O |  |  |  |  |  |  |  |
| AAI | O | O |  |  |  |  |  |  |  |
| VVI | O | O |  |  |  |  |  |  |  |

### AOO

In AOO mode the pacemaker must include a lower rate limit, an upper rate limit, atrial amplitude control, and atrial pulse width control.

### VOO

In VOO mode the pacemaker must include a lower rate limit, an upper rate limit, ventricular amplitude, and ventricular pulse width.

### AAI

In AAI mode the pacemaker must include a lower rate limit, an upper rate limit, atrial amplitude control, atrial pulse width control, atrial sensitivity, ARP, and PVARP.

### VVI

In VVI mode the pacemaker must include a lower rate limit, an upper rate limit, ventricular amplitude, ventricular pulse width, ventricular sensitivity, and VRP.

Hardware hiding will be used to map the pins of the microcontroller to the inputs and output of the pacemaker system.

### States

The permanent bradycardia state, the normal pacing state, should be available. All the pacing parameters in this normal state should also be used in the permanent brady state.

### Programmable Parameters

### Lower Rate Limit (LRL)

The number of generator pace pulses delivered (per minute) should be affected by following the requirements.

1. When Rate Hysteresis is disabled, the LRL shall define the longest allowable pacing interval.
2. In DXX or VXX modes, the LRL interval starts at a ventricular sensed or paced event.
3. In AXX modes, the LRL interval starts at an atrial sensed or paced event.

### Upper Rate Limit (URL)

The URL should be the maximum rate at which the paced ventricular rate will track sensed atrial events. URL interval is the minimum time between a ventricular event and the next ventricular pace.

### Ventricular Refractory Period (VRP)

The VRP should follow the programmed time interval following a ventricular event during which time ventricular senses shall not inhibit nor trigger pacing.

### Atrial Refractory Period (ARP)

ARP has to be in single chamber atrial modes, which is the programmed time interval following an atrial event during which time atrial events shall not inhibit nor trigger pacing.

### Post Ventricular Atrial Refractory Period (PVARP)

It must be available in modes with ventricular pacing and atrial sensing. It is the programmable time interval following a ventricular event when an atrial cardiac event shall not inhibit an atrial pace, and trigger a ventricular pace.

## Design decisions

A subsystem is used to map the pins inputting data for use in the program to their names as defined in Table 1 of Pacemaker Sheild Explained. Another subsystem is used to map the output pins to their names in the same table. This allows the variables used within the program to be called “ATR\_CMP\_DETECT” instead of D0 everywhere, which should make it more readable, and hide the software from the hardware.

## Simulink diagram and testing

Pt2:

1. List likely changes to requirements
2. List all design decisions likely to change
3. For each module:
   1. Describe purpose
   2. List public functions and parameters
   3. Describe black box behaviour
   4. Describe global variables (state variables)
   5. List private functions in module
   6. Describe internal behaviour of functions

# Part 2: Future flexibility and modules

## 2.1 Requirements likely to change

In the future, more modes will need to be added. Subsystems are used to encapsulate the different operating modes to make it easier to add new ones.

## 2.2 Design decisions likely to change

## 2.3 MIS and MID