Simulink Documentation

Pt1:  
1. List all requirements – they must be concise and disjoint

(1) Overall Pacemaker System

• Provides dual chamber, rate adaptive bradycardia pacing support  
• Provides historical data on device performance  
• Provides user diagnostics through brady analysis function

(2) Performance  
: Lead impedance, pacing threshold, P and R wave measurement, battery status, Temporary brady pacing, Motion sensor trending

(3) Device

• Should monitor and regulate a patient’s heart rate  
• Should programmable, single- and dual-chamber, rate-adaptive pacing, both permanent and temporary  
• Should output rate histograms (atrial and ventricular) and sensor output data

(4) Pulse Pacing (atrial and ventricular)

• Amplitude and width should be independently programmable  
• Rate sensing is used by bipolar electrodes and sensing circuit  
• Rate detection should be based on the measured cardiac cycle lengths of the sensed rhythm

(5) States

• Permanent: normal state and permanent brady state  
• Temporary: temporary brady state  
• Pace-Now: parameter value of VVI

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Lower Rate Limit | Amplitude | Pulse Width | Ventricular Refractory | Ventricular Sensitivity |
| 65 ppm +/- 8 ms | 5.0 V +/- 0.5 V | 1.00 ms +/- 0.02 ms | 320 ms +/- 8 ms. | 1.5 mV |

• Magnet: used during the Magnet Test  
• Power-On Reset (POR): parameter value of VVI

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Lower Rate Limit | Amplitude | Pulse Width | Ventricular Refractory | Ventricular Sensitivity |
| 65 ppm +/- 8 ms | 5.0 V +/- 0.5 V | 0.5 ms +/- 0.02 ms | 320 ms +/- 8 ms. | 1.5 mV |

4. Programmable Parameters

**Lower Rate Limit (LRL)** - number of generator pace pulses delivered per minute (atrium or ventricle)   
affected by:  
1. When Rate Hysteresis is disabled, the LRL shall define the longest allowable pacing interval.  
2. In DXX or VXX modes, the LRL interval starts at a ventricular sensed or paced event.  
3. In AXX modes, the LRL interval starts at an atrial sensed or paced event.

**Upper Rate Limit (URL)** - maximum rate at which the paced ventricular rate will track sensed atrial events. URL interval is the minimum time between a ventricular event and the next ventricular pace

**Ventricular Refractory Period (VRP) -** the programmed time interval following a ventricular event during which time ventricular senses shall not inhibit nor trigger pacing.

**Atrial Refractory Period (ARP)** - in single chamber atrial modes, arp is the programmed time interval following an atrial event during which time atrial events shall not inhibit nor trigger pacing

**Post Ventricular Atrial Refractory Period (PVARP)** - available in modes with  
ventricular pacing and atrial sensing. It is the programmable time interval following a ventricular event when an atrial cardiac event shall not 1. Inhibit an atrial pace. 2. Trigger a ventricular pace  
  
**Hysteresis -** hysteresis pacing shall result in a longer period following a sensed  
event before pacing. encourages self-pacing during exercise by waiting a  
little longer to pace after senses, hoping that another sense will inhibit the pace.  
To use hysteresis pacing:  
1. Hysteresis pacing must be enabled (not Off).  
2. The pacing mode must be inhibiting or tracking.  
3. The current pacing rate must be faster than the Hysteresis Rate Limit (HRL), which may be slower than LRL  
4. When in AAI mode, a single, non-refractory sensed atrial event shall activate hysteresis pacing.  
5. When in an inhibiting or tracking mode with ventricular pacing, a single, non-refractory sensed ventricular event shall activate hysteresis pacing

**Rate smoothing -** limit the pacing rate change that occurs due to precipitous changes in the intrinsic rate.  
Two programmable rate smoothing parameters shall be available to allow the cardiac cycle interval change to be a percentage of the previous cardiac cycle interval:  
1. Rate Smoothing Up  
2. Rate Smoothing Down  
The increase in pacing rate shall not exceed the Rate Smoothing Up percentage.  
The decrease in pacing rate shall not exceed the Rate Smoothing Down percentage.

# Part 1: Requirements and design

## Requirements

These are all the requirements for the Simulink implementation of the pacemaker and its modes.

The DCM will be used to select a permanent operating mode for the pacemaker at startup. At present, it will choose between the modes AOO, VOO, AAI, and VVI.

### AOO

In AOO mode the pacemaker must include a lower rate limit, an upper rate limit, atrial amplitude control, and atrial pulse width control.

### VOO

In VOO mode the pacemaker must include a lower rate limit, an upper rate limit, ventricular amplitude, and ventricular pulse width.

### AAI

In AAI mode the pacemaker must include a lower rate limit, an upper rate limit, atrial amplitude control, atrial pulse width control, atrial sensitivity, ARP, PVARP, hysteresis, and rate smoothing.

### VVI

In VVI mode the pacemaker must include a lower rate limit, an upper rate limit, ventricular amplitude, ventricular pulse width, ventricular sensitivity, VRP, hysteresis, and rate smoothing.

Hardware hiding will be used to map the pins of the microcontroller to the inputs and output of the pacemaker system.

## Design decisions

A subsystem is used to map the pins inputting data for use in the program to their names as defined in Table 1 of Pacemaker Sheild Explained. Another subsystem is used to map the output pins to their names in the same table. This allows the variables used within the program to be called “ATR\_CMP\_DETECT” instead of D0 everywhere, which should make it more readable, and hide the software from the hardware.

## Simulink diagram and testing

Pt2:

1. List likely changes to requirements
2. List all design decisions likely to change
3. For each module:
   1. Describe purpose
   2. List public functions and parameters
   3. Describe black box behaviour
   4. Describe global variables (state variables)
   5. List private functions in module
   6. Describe internal behaviour of functions

# Part 2: Future flexibility and modules

## 2.1 Requirements likely to change

In the future, more modes will need to be added. Subsystems are used to encapsulate the different operating modes to make it easier to add new ones.

## 2.2 Design decisions likely to change

## 2.3 MIS and MID